SESSION 15 – TAPA II
Emerging Memory Technologies II

Wednesday, June 16, 3:25 p.m.
Chairpersons: C. Dennison, Ovonyx
K. Sakamoto, AIST

15.1 — 3:25 p.m.

New Highly Scalable 3 Dimensional Chain FeRAM Cell with Vertical Capacitor, N. Nagel, R. Bruchhaus, K. Hornik, U. Egger, H. Zhuang, H.-O. Joachim, T. Röehr, G. Beitel, T.Ozaki* and I. Kunishima*, FeRAM Development Alliance, Yokohama, Japan, Infineon Technologies AG, Munich, Germany, *Toshiba Corporation, Yokohama, Japan

Ferroelectric random access memories (FeRAMs) combine non-volatility with fast access time and low operation voltage. A Chain FeRAM cell, which provides random access on top of a small NAND like structure, is successfully demonstrated with a 3 dimensional Vertical Capacitor for the first time. The Vertical Capacitor concept is highly scalable to feature sizes below 0.1μm with small cell sizes. This breakthrough opens up a new door for 3D high density FeRAM.

15.2 — 3:50 p.m.

Highly Reliable and Mass-Productive FRAM Embedded Smartcard Using Advanced Integration Technologies, H. J. Joo, Y. J. Song, H. H. Kim, S. K. Kang, J. H. Park, Y. M. Kang, E. Y. Kang, S. Y. Lee, H. S. Jeong and K. Kim, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

We developed FRAM embedded smartcard in which FRAM replace EEPROM and SRAM to improve the read/write cycle time and endurance of data memories in smartcard. Highly reliable sensing window for FRAM embedded smartcard was achieved by advanced integration technologies such as novel capacitor technology, multi-level encapsulating barrier layer (EBL) technology, and optimalinter-metallic dielectrics (IMD) technology.

15.3 — 4:15 p.m.

A 0.602 μm^2 Nestled Chain Cell Structure Formed By One Mask Etching Process For 64 Mbit FeRAM, H. Kanaya, K. Tomioka, T. Matsushita, M. Omura, T. Ozaki, Y. Kumura, Y. Shimojo, T. Morimoto, O. Hidaka, S. Shuto, H. Koyama, Y. Yamada, K. Osari, N. Tokoh, F. Fujisaki, N. Iwabuchi, N. Yamaguchi, T. Watanabe, M. Yabuki, H. Shinomiya, N. Watanabe, E. Itoh, T. Tsuchiya, K. Yamakawa, K. Natori, S. Yamazaki, K. Nakazawa, D. Takashima, S. Shiratake, S. Ohtsuki, Y. Oowaki, I. Kunishima and A. Nitayama, Toshiba, Yokohama, Japan

We have successfully developed a 0.602 um2 nestled 'Chain' FeRAM cell technology for 64Mbit FeRAM. In the 'Chain' FeRAM, a pair of capacitors on a same node can be nestled close to each other. A combination of a one mask etching process of ferro-electric capacitors and the nestled structure drastically scaled down the cell size to 0.602um2. The cell size was reduced to 32% of previous work. Signal window of 600mV was obtained by the nestled 'Chain' FeRAM structure after full integration of three-metal CMOS technology. (Keywords : Chain, FeRAM, W-plug, Ir, IrO2, and one mask etching)

15.4 — 4:40 p.m.

Ultra-High Speed Direct Tunneling Memory (DTM) for Embedded RAM Applications, K.Tsunoda, A.Sato, H.Tashiro, K.Ohira, T.Nakanishi, H.Tanaka and Y.Arimoto, Fujitsu Laboratories, Ltd., Atsugi, Japan

Direct Tunneling Memory (DTM) with ultra-thin tunnel oxide and novel depleted floating gate has been demonstrated for embedded RAM applications. Fast programming (<10ns) at low voltage, together with its excellent charge retention (>10s) and large threshold voltage difference (>1.3V), has been achieved by utilizing the band bending at the poly-Si/oxide interface in charge retention period. Depleted floating gate is also effective to suppress the degradation of program/erase speed caused by the gate re-oxidation process.